VERIFICATION OF A TRANSLATION

I, Tetsuo AKIYOSHI, of 5th Floor, Shintoshicenter Bldg., 24-1, Tsurumaki 1-chome, Tama-shi, Tokyo 206-0034 Japan, declare that I am well acquainted with both the Japanese and English languages, and that the attached is an accurate translation, to the best of my knowledge and ability, of the Japanese Patent Application No. 2003-402232 filed on December 1, 2003.

Signature 

Tetsuo AKIYOSHI

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[Inventor]	
[Address or Residence]	c/o Matsushita Electric Industrial Co., Ltd. 1006, Oaza Kadoma, Kadoma-shi, Osaka, Japan 571-8501
[Name]	Yoshito SHIMIZU
[Inventor]	
[Address or Residence]	c/o Matsushita Electric Industrial Co., Ltd. 1006, Oaza Kadoma, Kadoma-shi, Osaka, Japan 571-8501
[Name]	Noriaki SAITO
[Applicant for Patent]	
[Identification Number]	000005821
[Name]	MATSUSHITA ELECTRIC INDUSTRIAL CO., LTD.
[Agent]	
[Identification Number]	100105050
[Patent Attorney]	
[Name]	Kimihito WASHIDA
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[TITLE OF THE INVENTION]

RECEPTION APPARATUS AND RECEPTION METHOD

CLAIMS

[Claim 1] A reception apparatus comprising:

a reception quality measurement section that finds a measurement value indicating reception quality from a received signal;

a gain setting section that sets a gain for amplifying the received signal of transmit power estimated in a predetermined reception period to a reference value for each time slot, based on transmit power information comprising information indicating transmit power of each time slot at a communicating party and said measurement value;

a gain control section that performs gain control over the received signal before said reception period at a maximum gain among gains set in said reception period by said gain setting section, and that performs gain control over the received signal of each time slot at a gain less than or equal to said maximum gain set in said reception period by said gain setting section; and

a voltage calibration section that calibrates offset voltage of the received signal before said reception period and after the gain control at said maximum gain in said gain control section.

[Claim 2] The reception apparatus according to claim 1, wherein said gain setting section subtracts the transmit power of said transmit power information from said measurement value for each time slot and estimates the transmit power of each time slot.

[Claim 3] The reception apparatus according to one of claim 1 and claim 2, wherein:

upon performing gain control over the received signal in said gain control section through a plurality of stages, said gain setting section sequentially sets gains such that the gain in an earlier one of two consecutive stages is greater than or equal to the gain in a later one of said consecutive stages; and

by performing gain control of a received signal for each of said stages at a gain for each of said stages set by said gain estimation section,

said gain control section performs gain control of the received signal at said maximum gain before said reception period and performs gain control of the received signal of each time slot at a gain less than or equal to said maximum gain in said reception period.

[Claim 4] A communication terminal apparatus comprising the reception apparatus according to one of claims 1 to 3.

[Claim 5] A reception method comprising the steps of:

finding a measurement value indicating reception quality from a received signal;

setting a gain for amplifying the received signal of transmit power estimated in a predetermined reception period to a reference value for each time slot, based on transmit power information comprising information indicating transmit power of each time slot at a communicating party and said measurement value;

performing gain control over the received signal before said reception period at a maximum gain among gains set in said reception period;

calibrating offset voltage of the received signal before said reception period and after the gain control at said maximum gain; and

performing gain control over the received signal of the calibrated offset voltage for each time slot at a gain less than or equal to said maximum gain set in said reception period.

[DETAILED DESCRIPTION OF THE INVENTION]

[Technical Field of the Invention]

[0001] The present invention relates to a reception apparatus and a reception method, and more particularly, to a reception apparatus and a reception method for use in a system where transmit power of transmission signals varies by downlink transmit power control.

[Background Art]

[0002] In cellular phone services in recent years, in addition to voice calls, a demand for data communication is expanding with an increasing number of subscribers (mobile stations), and therefore it is important to efficiently use resources such as frequency channels and improve communication speed. For example, in a GSM (Global System for Mobile communications) system which is becoming popular mainly in Europe and Asian regions, services corresponding to high-speed communication called "GPRS" (General Packet Radio Service) have started. In GPRS, with respect to a link between mobile stations and a base transceiver station, instead of allocating dedicated frequency channels to a specific mobile station, the same frequency channel is shared by a plurality of mobile stations, and, when data to be transmitted to the other party exists in either the mobile station or base transceiver station, time slots are allocated to a specific mobile station every time. This scheme improves utilization efficiency of frequency channels. Moreover, by using a multi-slot transmission scheme which allocates a plurality of time slots in a data frame to the same mobile station, improvement of downlink speed from the base transceiver station to the mobile station is realized.

[0003] However, when the same frequency channel is shared by a plurality of mobile stations in a cell covered by a specific base transceiver station, the distance between the base transceiver station and each mobile station differs from one mobile station to another, and therefore it is necessary for the base transceiver station to carry out transmission to each mobile station with transmit power so that the farthest mobile station in the cell can receive data in predetermined quality, and, in this case, unnecessary power is radiated to the cell and interference with cells covered by adjacent base transceiver stations becomes a problem.

[0004] Therefore, an interference measures in GPRS will be explained

using FIG.9.FIG.9 is a GSM network configuration.

[0005] In FIG.9, a GSM network is configured with telephone network 901 of fixed-line phones, mobile services switching center (MSC) 902, base station controllers (BSC) 903, 904, 905, base transceiver stations (BTS) 906, 907, 908 and mobile stations (MS) 911, 912, 913, 914, 915 which exist in respective cells 909, 910 covered by base transceiver stations 907, 908.

[0006] The GSM system is provided with at least one mobile services switching center 902 and mobile services switching center 902 is connected to telephone network 901.A plurality of base station controllers 903, 904, 905 are provided below mobile services switching center 902 and at least one base transceiver station 906, 907, 908 is provided below base station controllers 903, 904, 905 and communication is carried out between the base transceiver stations. In FIG.9, communication is possible, for example, between mobile station 912 in cell 909 and mobile station 914 in cell 910 or between mobile station 913 and telephone network 901. When transmission is performed to all the mobile stations with the same output power when the distances between mobile stations 911, 912, 913 in cell 909 and base transceiver station 907 differ from one another, transmit power is set based on the farthest mobile station, and therefore power which would be unnecessary under normal conditions is sent to the same frequency channels, which results in a problem of interference against adjacent cells. Thus, GPRS realizes downlink transmit power control ("base transceiver station power control") to corresponding mobile stations according to the distance between base transceiver station 907 and mobile stations 911, 912, 913.

Specific examples of transmit power control include a method of reporting a decrement value (0 to 30 dB) of transmit power from a broadcast control channel ("BCCH") to a mobile station using a P0 parameter in a resource allocation message of the downlink which is transmitted on a control channel. BCCH is an important channel which all mobile stations existing in the cell should refer to and is transmitted with a sufficient transmission level (POWbcch: a fixed value) that even the mobile station at the maximum distance from the base transceiver station can reproduce data reliably.

[0007] Also, with a direct conversion receiver which is a mainstream as a reception section configuration of the mobile station at present, DC offset

voltage is produced due to gain switching in accordance with changes of reception field intensity and there is a possibility that a receiver may be saturated, and therefore it is necessary to perform gain switching immediately before receiving demodulated data and then calibrate the DC offset voltage at high speed (for example, see Patent Document 1.)

[0008] FIG.10 is a block diagram of conventional DC offset voltage calibration circuit 1000. In FIG.10, DC offset voltage calibration circuit 1000 is configured with low noise amplifier 1001, quadrature demodulator 1002 that converts the frequency of a radio frequency to a baseband, 90-degree phase shifter 1003 that outputs 2 signals having a phase difference of 90 degrees for quadrature demodulator 1002, analog baseband circuit 1004 made up of variable gain amplifiers and low pass filters, voltage calibration circuit 1005 that calibrates DC offset voltage of analog baseband circuit 1004 and digital signal processing section 1006 that converts the signal received from analog baseband circuit 1004 to a voice signal or data signal and transmits a calibration start signal to voltage calibration circuit 1005. Voltage calibration circuit 1005 executes calibration operation for a certain period using a calibration start signal as a trigger immediately before the frame and pauses during the frame. Furthermore, in the calibrating period, voltage calibration circuit 35 separates a capacitor from the signal line to improve the calibration response speed.

Patent Document 1: Japanese Patent Application Laid-Open No.2001-211098

[Disclosure of Invention]

[Problems to be Solved by the Invention]

[0009] However, though the conventional reception apparatus and reception method execute DC offset voltage calibration in frame units, such a case where the base transceiver station executes transmit power control is not assumed. That is, when reception field intensity differs between time slots in the same frame according to base transceiver station power control, each mobile station executes gain switching such that the signal level falls within a linear operation range of the receiver, but there is a problem that offset voltage that is newly generated due to high-speed gain switching is amplified by an amplifier located in circuit later than the place where the offset voltage is generated and leads to saturation and

sensitivity degradation of the receiver.

[0010] Furthermore, when performing transmit power control, the conventional apparatus needs to perform gain switching of the mobile station reception section during a guard time of approximately 30[us] provided at the rearmost of each time slot to prevent saturation and sensitivity degradation of the receiver and realize accurate demodulation. However, if offset voltage calibration is performed every time after the gain is switched to a desired value immediately before the time slot during which demodulation is performed, there is a problem that the amount of current consumption at the calibration circuit increases.

[0011] In view of the above, it is therefore an object of the present invention to provide a reception apparatus and reception method capable of preventing saturation and sensitivity degradation of the receiver and calibrating offset voltage without increasing current consumption when base transceiver station power control is performed.

[Means for Solving the Problems]

[0012] The reception apparatus of the present invention adopts a configuration having: a reception quality measurement section that finds a measurement value indicating reception quality from a received signal; a gain setting section that sets a gain for amplifying the received signal of transmit power estimated in a predetermined reception period to a reference value for each time slot, based on transmit power information comprising information indicating transmit power of each time slot at a communicating party and said measurement value; a gain control section that performs gain control over the received signal before said reception period at a maximum gain among gains set in said reception period by said gain setting section, and that performs gain control over the received signal of each time slot at a gain less than or equal to said maximum gain set in said reception period by said gain setting section; and a voltage calibration section that calibrates offset voltage of the received signal before said reception period and after the gain control at said maximum gain in said gain control section.

[0013] With this configuration, gain control is performed for a received signal in a reception period at a gain less than or equal to a gain at which gain control of a received signal is performed upon offset voltage calibration before the reception period, it is possible to suppress an

amplification of remaining offset voltage that are not calibrated completely upon offset voltage calibration, so that it is possible to prevent saturation and sensitivity degradation of a receiver and calibrate offset voltage without increasing current consumption even when transmit power control is performed.

[0014] The reception apparatus of the present invention adopts a configuration in which the gain setting section subtracts the transmit power of the transmit power information from the measurement value for each time slot and estimates the transmit power of each time slot.

[0015] With this configuration, even when transmit power control is performed, accurate gain switching can be realized during a reception period, in addition to the above effect.

[0016] The reception apparatus of the present invention adopts a configuration in which: upon performing gain control over the received signal in said gain control section through a plurality of stages, said gain setting section sequentially sets gains such that the gain in an earlier one of two consecutive stages is greater than or equal to the gain in a later one of said consecutive stages; and by performing gain control of a received signal for each of said stages at a gain for each of said stages set by said gain estimation section, said gain control section performs gain control of the received signal at said maximum gain before said reception period and performs gain control of the received signal of each time slot at a gain less than or equal to said maximum gain in said reception period.

[0017] With this configuration, in addition to the above effect, a gain control section employs a multi-stage configuration, so that it is reliably possible to suppress amplification of remaining offset voltage that are not calibrated completely upon DC offset voltage calibration.

[0018] The communication terminal apparatus of the present invention adopts a configuration having one of the reception apparatuses described above.

[0019] With this configuration, gain control is performed for a received signal in a reception period at a gain less than or equal to a gain at which gain control of a received signal is performed upon offset voltage calibration before the reception period, it is possible to suppress an amplification of remaining offset voltage that are not calibrated completely upon offset voltage calibration, so that it is possible to prevent saturation and sensitivity degradation of a receiver and calibrate offset

voltage without increasing current consumption even when transmit power control is performed.

[0020] The reception method of the present invention includes the steps of: finding a measurement value indicating reception quality from a received signal; setting a gain for amplifying the received signal of transmit power estimated in a predetermined reception period to a reference value for each time slot, based on transmit power information comprising information indicating transmit power of each time slot at a communicating party and said measurement value; performing gain control over the received signal before said reception period at a maximum gain among gains set in said reception period; calibrating offset voltage of the received signal before said reception period and after the gain control at said maximum gain; and performing gain control over the received signal of the calibrated offset voltage at a gain less than or equal to said maximum gain set in said reception period.

[0021] With this method, gain control is performed for a received signal in a reception period at a gain less than or equal to a gain at which gain control of a received signal is performed upon offset voltage calibration before the reception period, it is possible to suppress an amplification of remaining offset voltage that are not calibrated completely upon offset voltage calibration, so that it is possible to prevent saturation and sensitivity degradation of a receiver and calibrate offset voltage without increasing current consumption even when transmit power control is performed.

Advantageous Effect of the Invention

[0022] According to the present invention, it is possible to prevent saturation and sensitivity degradation of a receiver and calibrate offset voltage without increasing current consumption when base transceiver station power control is performed in multi-slot transmission.

[Best Mode for Carrying Out the Invention]

[0023] An essence of the present invention is to set a gain for each time slot in a predetermined reception period (1 frame) before the reception period, perform gain control of a received signal before a reception period at the maximum gain out of the set gains, calibrate offset voltage of the received signal after the gain control at the maximum gain and before the

reception period and perform gain control of the received signal of the calibrated offset voltage at a gain equal to or below the maximum gain set in each time slot during the reception period.

[0024] Now, embodiments of the present invention will be described in detail with reference to the accompanying drawings.

[0025] (Embodiment 1)

FIG.1 is a block diagram showing the configuration of reception apparatus 100 according to Embodiment 1 of the present invention. Reception apparatus 100 in FIG.1 is a direct conversion reception apparatus.

[0026] Low noise amplifier 101 amplifies a received signal and outputs the result to quadrature demodulator 103 via capacitor 102 that removes the DC component.

[0027] Quadrature demodulator 103 has mixer 103a and mixer 103b, converts the frequency of the received signal inputted from capacitor 102 from a radio frequency to a baseband, outputs the baseband from mixer 103a to analog baseband circuit 105a and at the same time outputs the baseband from mixer 103b to analog baseband circuit 105b.

[0028] Phase shifter 104 generates two signals which have a phase difference of 90 degrees mutually from a local oscillation signal inputted from a local oscillation source (not shown) and outputs the two signals to mixer 103a and mixer 103b of quadrature demodulator 103 respectively.

[0029] Analog baseband circuits 105a, 105b are composed of a variable gain amplifier and a low pass filter and when the reception field intensity changes from a sensitivity point to an intense electric field, analog baseband circuits 105a, 105b reduce the gain of the received signal inputted from quadrature demodulator 103 one by one starting from the later circuits based on the control of gain control circuit 110 and outputs the received signal to digital signal processing section 106.In this case, analog baseband circuits 105a, 105b calibrate the DC offset voltage of the received signal based on the control of voltage calibration circuit 111. Analog baseband circuit 105a and analog baseband circuit 105b have the same configuration. Details of analog baseband circuits 105a, 105b will be described later.

[0030] Digital signal processing section 106 reproduces transmission data from the base transceiver station based on the received signal inputted from analog baseband circuits 105a, 105b and displays data on a display section (not shown) or outputs voice to a speaker (not shown).Furthermore, digital signal processing section 106 outputs a calibration start signal to start calibration of a DC offset voltage at

predetermined timing to voltage calibration circuit 111. Furthermore, digital signal processing section 106 measures an RSSI (Received Signal Strength Indicator) from the received signal of BCCH which is transmitted from the base transceiver station and outputs the measurement result to field intensity measurement section 108. Moreover, digital signal processing section 106 outputs demodulated data to transmit power information extraction section 107.

[0031] Transmit power information extraction section 107 extracts transmit power information (e.g., P0 parameter) for each time slot from the demodulated data inputted from digital signal processing section 106 and outputs the result to gain setting section 109.

[0032] Field intensity measurement section 108 is a reception quality measurement section and reduces the influence of fading using a publicly known method from the measurement result of the RSSI inputted from digital signal processing section 106, obtains the reception field intensity of a received signal of BCCH which becomes the control reference of base transceiver station transmit power for each time slot and outputs the obtained information of the reception field intensity to gain setting section 109.

[0033] Gain setting section 109 estimates the reception field intensity of each time slot from the information of the reception field intensity of BCCH which becomes the control reference of base transceiver station transmit power for each time slot inputted from field intensity measurement section 108 and transmit power information at each time slot inputted from transmit power information extraction section 107 and calculates a gain set value according to the estimated reception field intensity. For example, gain setting section 109 sets a gain for amplifying the received signal of the transmit power estimated by subtracting an incremented/decremented value of the base transceiver station transmit power acquired from the transmit power information from the reception field intensity of BCCH to a reference value for each time slot. Then, gain setting section 109 outputs gain information which is information of the gains of the respective set time slots to gain control circuit 110.

[0034] Gain control circuit 110 is a gain control section and extracts a maximum gain from the gain information inputted from gain setting section 109 and outputs the result to analog baseband circuits 105a, 105b

as a set gain for a calibration of the DC offset voltage. Furthermore, gain control circuit 110 temporarily stores the gain set value which corresponds to each time slot, sequentially outputs the gain set values corresponding to the respective time slots to analog baseband circuits 105a, 105b immediately before the respective time slots and performs gain control. Furthermore, gain control circuit 110 performs gain control every stage of analog baseband circuits 105a, 105b having the multi-stage circuit configuration. The gain setting method for the calibration of DC offset voltage will be described later.

[0035] When a calibration start signal is inputted at predetermined timing from digital signal processing section 106, voltage calibration circuit 111, which is a voltage calibration section, performs calibration of the DC offset voltage produced in the received signal of analog baseband circuits 105a, 105b. In this case, voltage calibration circuit 111 calibrates the DC offset voltage every stage of analog baseband circuits 105a, 105b having a multi-stage circuit configuration.

[0036] Next, the configurations of analog baseband circuits 105a, 105b will be explained using FIG.2.FIG.2 is a block diagram showing the configuration of analog baseband circuit 105a.Since the configurations of analog baseband circuit 105a and analog baseband circuit 105b are the same, explanations of the configuration of analog baseband circuit 105b will be omitted.

[0037] Analog baseband circuit 105a is configured with multi-stage circuits in 3 stages; variable gain amplifier 201 and filter 202 constituting first stage circuit 207, variable gain amplifier 203 and filter 204 constituting second stage circuit 208 and variable gain amplifier 205 and filter 206 constituting third stage circuit 209.First stage circuit 207 is a circuit before second stage circuit 208 and third stage circuit 209, second stage circuit 208 is a circuit after first stage circuit 207 and before third stage circuit 209, and third stage circuit 209 is a circuit after first stage circuit 207 and second stage circuit 208.

[0038] Variable gain amplifier 201 calibrates the DC offset voltage of the received signal inputted from mixer 103a based on the control of voltage calibration circuit 111.Furthermore, variable gain amplifier 201 sets the received signal inputted from mixer 103a to a predetermined gain based on the control of gain control circuit 110 and outputs the result to filter 202.

[0039] Filter 202 allows only a predetermined band of the received signal inputted from variable gain amplifier 201 to pass, and outputs the result to variable gain amplifier 203.

[0040] Variable gain amplifier 203 calibrates the DC offset voltage of the received signal inputted from filter 202 based on the control of voltage calibration circuit 111.Furthermore, variable gain amplifier 203 sets the received signal inputted from filter 202 to a predetermined gain based on the control of gain control circuit 110, and outputs the result to filter 204.

[0041] Filter 204 allows only a predetermined band of the received signal inputted from variable gain amplifier 203 to pass, and outputs the result to variable gain amplifier 205.

[0042] Variable gain amplifier 205 calibrates the DC offset voltage of the received signal inputted from filter 204 based on the control of voltage calibration circuit 111.Furthermore, variable gain amplifier 205 sets the received signal inputted from filter 204 to a predetermined gain based on the control of gain control circuit 110, and outputs the result to filter 206.

[0043] Filter 206 allows only a predetermined band of the received signal inputted from variable gain amplifier 205 to pass, and outputs the result to digital signal processing section 106.In this way, analog baseband circuits 105a, 105b allow the received signal to pass through first stage circuit 207, second stage circuit 208 and third stage circuit 209, thereby eliminating unnecessary band components and amplifying the received signal so as to obtain the gain set by digital signal processing section 106.

[0044] Next, the operation of reception apparatus 100 will be explained using FIG.3 to FIG.5.FIG.3 shows the downlink frame configuration in GPRS, FIG.4 shows the configuration of consecutive downlink time slots in GPRS and FIG.5 is a schematic view showing transmit power when transmit power control is performed by the base transceiver station in multi-slot transmission.

[0045] FIG.3 shows the frame configurations of frame #301 and frame #302 which are predetermined reception periods. In FIG.3, the horizontal axis is time. Furthermore, in FIG.3, frame #301 contains downlink information for a desired mobile station and frame #302 is a frame immediately before frame #301.Furthermore, frequency channels #303, #304, #305 are channels of different downlink frequencies and time slots #310 to #317 are eight time slots which make up frame #301.On the other hand, time slot #318 is the rearmost time slot of frame #302 and a free time

space which contains no effective data and which is called "guard time" is provided at the rearmost of each time slot.

[0046] FIG.4 shows the configurations of time slot #318 and time slot #310, where time slot #318 has guard time #401 at the rearmost and time slot #310 has guard time #402 at the rearmost. Frame #301 is received later than frame #302 and the time slots and the frames are received later in accordance with described in the right in FIG.3 and FIG.4.

[0047] Also, in FIG.5, the horizontal axis is time and the vertical axis is the transmit power intensity transmitted by a specific base transceiver station.In FIG.5, as an example of base transceiver station power control in multi-slot transmission, a case is assumed where data in time slots #310, #311, #312 and #313 are allocated to mobile stations #501, #502, #503 respectively. Also, mobile stations #501 to #503 share time slots #310 to #313, and perform demodulation of time slots #310 to #313 for receiving data for those mobile stations. Therefore, mobile stations #501, #502 receive time slot #310, mobile station #502 receives time slot #311 and mobile stations #502, #503 receive time slots #312, #313.Also, suppose that FIG.5 shows transmit power intensity at the base transceiver station antenna output terminal for time slots #310, #311, #312 and #313, and, among the time slots executing downlink transmission out of time slots #310, #311, #312, #313, #314, #315, #316, #317 of frame #301, the transmit power at time slot #310 is the largest and the transmit power at time slot #311 is the smallest.

[0048] First, digital signal processing section 106 measures RSSI of BCCH transmitted from the base transceiver station communicating with reception apparatus 100 in time slots other than the downlink time slots and uplink time slot allocated to reception apparatus 100 in frame #302 or an idle frame which contains no effective data (not shown in FIG.7.) Field intensity measurement section 108 reduces the influence of fading using a publicly known technology from the RSSI measurement value obtained before frame #301 and obtains the reception field intensity (POWbcch) of BCCH which becomes a control reference of the base transceiver station transmit power for each time slot in frame #301 and outputs the result to gain control circuit 110.

[0049] When the transmit power information of time slot #310 is P0(#310), the transmit power information of time slot #311 is P0(#311), the transmit power information of time slot #312 is P0(#312), the transmit

power information of time slot #313 is P0(#313) and P0(#312)=P0(#313) as the transmit power information of the respective time slots inputted to gain control section 110 from transmit power information extraction section 107, gain control section 110 performs calculations of POWbcch-P0(#310), POWbcch-P0(#311), POWbcch-P0(#312) using POWbcch inputted from field intensity measurement section 110 as a reference. When gain switching is performed in guard time #401 immediately before each time slot in frame #301, the set gain of each corresponding time slot is obtained from the calculation result of POWbcch-P0(#310), POWbcch-P0(#311), POWbcch-P0(#312).Furthermore, as the set gain for the calibration of the DC offset voltage carried out in guard time #401 immediately before frame #301, a maximum gain (Gmax[dB]) in frame #301 is obtained using a set gain when the P0 parameter is a maximum. For example, in guard time #401 provided at the rearmost of time slot #318 in frame #302 in FIG.3, the P0 parameter which is the transmit power information of time slots #310 to #317 in frame #301 is compared. As a result of the comparison, since the P0 parameter which corresponds to time slot #311 is the largest, gain control circuit 110 selects the gain set value which corresponds to time slot #311 and sets it as gain information (Gmax[dB]) for the calibration of the DC offset voltage.

[0050] Then, in guard time #401, gain control circuit 110 outputs gain information (Gmax[dB]) to analog baseband circuits 105a, 105b and sets a gain upon the calibration and after that, a calibration start signal is transmitted from digital signal processing section 106. Voltage calibration circuit 111 realizes a calibration operation in the above guard time using the calibration start signal as a trigger and then pauses in a period other than the guard time (not shown) at the rearmost of time slot #317 in frame #301.After that, in guard time #401, gain control circuit 110 outputs the gain information set to a desired value (G1[dB]) for time slot #310 to analog baseband circuits 105a, 105b and thereby sets the gain of time slot #310.Then, after the gain setting at analog baseband circuits 105a, 105b is completed, time slot #310 is received. After the reception of time slot #310 is completed, in a guard time (not shown) provided at the rearmost of time slot #310, gain control circuit 110 outputs the gain information set to a desired value (G2[dB]) for time slot #311 and sets gains of analog baseband circuits 105a, 105b.Hereinafter until reception of

time slot #313 is completed, similar operations are repeated. In the guard time included in time slot #317 at the rearmost of frame #301, calibration operation of the DC offset voltage is carried out following the same procedure as that carried out immediately before frame #301.The operation during frame reception after that is the same as the operation upon the reception of frame #301 and explanations thereof will be omitted.

[0051] According to the studies in the process leading to the present invention, when the reception field intensity changes from the sensitivity point to the intense electric field like analog baseband circuits 105a, 105b of reception apparatus 100--, in the case where a gain is reduced after calibration of the DC offset voltage is performed with a specific gain setting in the gain switching configuration in which a gain is reduced sequentially starting from the later circuit-- the remaining DC offset voltage which is the offset voltage left in the received signal without being calibrated does not increase substantially. Therefore, offset voltage calibration is performed with the maximum gain setting in frame #301 in guard time #401 included in time slot #318 immediately before frame #301 of FIG.3, and consequently it is possible to say that the remaining offset voltage does not increase substantially even if gains are switched between time slots in frame #301. The reason will be explained below.

[0052] Means for realizing variable gains of variable gain amplifiers 201, 203, 205 of analog baseband circuits 105a, 105b includes a method of switching the ratio of the resistance value at the input section or the output section of variable gain amplifiers 201, 203, 205.

[0053] When only variable gain amplifier 201 is focused, if the voltage gain of variable gain amplifier 201 is G3[dB] and DC offset voltage ($\Delta V0$) occurs at the output of variable gain amplifier 201, the DC offset voltage of the input section of variable gain amplifier 201 is expressed as shown in Expression (1).

[0054]

$$\frac{\Delta V0}{10^{\frac{G3}{20}}} \qquad (1)$$

[0055] There is also a method of making a current (correction current) flow near the resistor of the input section of variable gain amplifier 201 from the outside at voltage calibration circuit 111 and canceling the DC

offset voltage using voltage drop effect caused by the correction current and the input resistance.

[0056] Here, there are three methods of switching the voltage gain of variable gain amplifier 201 from G3[dB] to G4[dB]: namely, the method of making input resistance variable, the method of making output resistance variable and the method of making both input resistance and output resistance variable.

[0057] Since the above voltage drop is calculated by multiplying the input resistance value of variable gain amplifier 201 and the correction current, the gain switching method of making input resistance variable makes the above voltage drop variable, and a remaining offset voltage of the offset voltage occurs at the input section of variable gain amplifier 201.Then. the remaining offset voltage of the input section of variable gain amplifier 201 is amplified by variable gain amplifier 201 by the gain and makes the calibration operation invalid.

[0058] On the other hand, it is preferable to use the gain switching method of making output resistance variable to prevent the occurrence of the above residual offset voltage. In this case, since the input resistance value is invariable, the above voltage drop ideally maintains a fixed value, no remaining offset occurs at the input section even if the gain is switched and "the offset voltage at the output section of variable gain amplifier 201 = the offset voltage of the input section of variable gain amplifier 201 × the gain of variable gain amplifier 201," the offset voltage of the output section of variable gain amplifier 201 becomes "0" even if gain switching is performed and the voltage gain becomes G4[dB].However, even when the method of making output resistance variable is used, a voltage drop at the input resistance section of the input section of variable gain amplifier 201 may deviate from the ideal condition due to correction current temperature characteristic, and, in this case, a problem occurs which is similar to the case where the method of making input resistance variable is used. In the method of making both the input resistance and the output resistance of variable gain amplifier 201 variable, the influence of both the above method of making input resistance variable and the method of making output resistance variable appear.

[0059] Thus, as the method of preventing the calibration operation at the input section of variable gain amplifier 201 from becoming invalid due to the gain switching, there is a method of switching the gain only in the

direction in which the gain is lower upon gain switching than the gain upon the calibration of the offset voltage. Since "the offset voltage at the output section of variable gain amplifier 201 = the offset voltage of the input section of variable gain amplifier 201 × the gain of variable gain amplifier 201," it is possible to further suppress the occurrence of offset voltage caused by gain switching as the gain after the gain switching is lower, and therefore it is effective as a method of preventing the calibration operation at the input section of variable gain amplifier 201 from becoming invalid due to gain switching. This method is of course effective for variable gain amplifiers 203, 205, too.

[0060] Next, in the case where analog baseband circuits 105a, 105b have a multi-stage circuit configuration, the method whereby the gain is switched only in the direction in which the gain is lower upon gain switching than the gain upon the calibration of the offset voltage will be explained using FIG.2, FIG.6 and FIG.7.FIG.6 and FIG.7 show gain distribution of variable gain amplifiers 201, 203, 205 at analog baseband circuits 105a and 105b and a total gain of analog baseband circuits 105a and 105b when the gains are set.FIG.6 and FIG.7 show examples where the point at which the total gain is 15[dB] is a sensitivity point and the electric field gradually becomes more intensive in accordance with the total gain approaching 0[dB] from 15[dB].

[0061] In this case, even if the gain of the received signal outputted from analog baseband circuits 105a, 105b falls below the gain upon a calibration of an offset voltage, the gains of variable gain amplifiers 201, 203, 205 of the respective stages are not necessarily switched in the direction in which the gain is reduced.

[0062] When, for example, the maximum gain required for analog baseband circuits 105a, 105b is 15[dB] and the minimum gain is 0[dB], if the total gain of analog baseband circuits 105a, 105b changes from 10[dB] to 5[dB]--that is, when transmit power information extraction section 107 estimates a maximum set gain for each frame and sets 10[dB] as the gain for the calibration of the offset voltage and a set gain of 5[dB] is necessary within a desired time slot--the gain of variable gain amplifier 203 is on the increase and the remaining offset voltage may expand.

[0063] On the other hand, in the case of FIG.7, if the total gain decreases, the gains of variable gain amplifiers 201, 203, 205 are fixed or on the decrease, and it is possible to restrain the expansion of the remaining

offset voltage.

[0064] When the maximum set gain of each variable gain amplifier is greater in the actual product or when a variable gain amplifier is further connected after the variable gain amplifier 205, a big problem occurs due to the remaining offset voltage of variable gain amplifier 203. Therefore, it is desirable to set a gain upon the offset voltage calibration of variable gain amplifiers 201, 203, 205 of the respective stages so that the gain is sequentially reduced from the later circuit as shown in FIG.7.

[0065] In this way, according to this Embodiment 1, in the frame immediately before frame #301, a maximum gain in frame #301 is estimated based on the maximum value extracted from the transmit power information reported from the base transceiver station, gain control is performed upon the calibration of the DC offset voltage at the estimated maximum gain, and the set gain in the case of gain control upon the reception operation after the completion of the calibration of the DC offset voltage is made lower than the set gain in the case of gain control upon the calibration of the DC offset voltage. Therefore it is possible to minimize the influence of the remaining offset voltage in gain control in the reception operation. This makes it possible to prevent saturation and sensitivity degradation of the receiver even when transmit power control is performed in multi-slot transmission and calibrate the offset voltage without increasing current consumption.

[0066] (Embodiment 2)

FIG.8 shows a time slot of a received signal in GPRS received by the reception apparatus of this Embodiment 2.The reception apparatus in this Embodiment 2 has the same configuration as that in FIG.1 and detailed explanations thereof will be omitted.

[0067] In FIG.8, the time slot of the received signal in GPRS is composed of header field 801 and data field 802.

[0068] Next, the operation of the reception apparatus will be explained using FIG.1 and FIG.3.In GPRS, there is a possibility that downlink power control may be realized using a P0 parameter in the control channel and PR parameter in header field 801 in the corresponding time slot.According to the GSM specification "Digital cellular telecommunications system (Phase 2+); Radio subsystem link control (3GPP TS 05.08 ver 8.16.0 Release 1999)", a mobile station receiver is required to satisfy the GSM specification "Digital cellular telecommunications system (Phase 2+);

Radio transmission and reception (3GPP TS 05.05 version 8.9.0 Release 1999)" up to a maximum of 10[dB]in multi-slot transmission with respect to power control using PR parameter.

[0069] Therefore, when power control using PR parameter is performed in the cell where the subject mobile station exists, gain control circuit 110 estimates a maximum gain (Gmax[dB]) in frame #301 using a set gain when the P0 parameter reported from the base transceiver station before the frame is a maximum.

[0070] Moreover, gain control circuit 110 generates Gmax+10[dB] as gain information based on set maximum gain Gmax.But, when Gmax+10[dB] is greater than the maximum total gain (Gtotal[dB]) of analog baseband circuits 105a, 105b, Gtotal[dB] is regarded as gain information. The rest of the operations are the same as in above Embodiment 1 and explanations thereof will be omitted.

[0071] In this way, according to this Embodiment 2, in addition to the advantage of above Embodiment 1, a maximum gain in frame #301 is estimated in frame #302 immediately before frame #301 based on the transmit power information reported from the base transceiver station and a gain higher than the estimated maximum gain by 10[dB] is set as the gain for the calibration of a DC offset voltage. Therefore it is possible to prevent saturation and sensitivity degradation of the receiver even when more efficient transmit power control satisfying the GSM specification is performed, and perform the offset voltage calibration without increasing current consumption.

[0072] In above Embodiment 1 and Embodiment 2, analog baseband circuits 105a, 105b are assumed to be constructed of multi-stage circuits having 3 stages, but the present invention is not limited to this and is applicable to multi-stage circuits having stages other than 3 stages, a circuit constructed of only one variable gain amplifier or constructed of one gain amplifier and one filter. Furthermore, Embodiment 1 and Embodiment 2 assume that a maximum set gain at each time slot of the next 1 frame is estimated in a guard time of the time slot at the rearmost of each frame, but the present invention is not limited to this, and, it is also possible to estimate a maximum set gain in a plurality of the following frames for every plurality of frames or for every plurality of time slots or estimate a maximum gain at a plurality of the following time slots. Furthermore, above Embodiment 1 and Embodiment 2 assume that a

maximum gain is estimated from a maximum value of a P0 parameter in frame #302 immediately before frame #301, but the present invention is not limited to this and if transmit power information is received in frames before frame #302, it is possible to estimate a maximum gain from a maximum value of the P0 parameter in an arbitrary frame before frame #302 after receiving transmit power information.Furthermore, reception apparatuses 100 of above Embodiment 1 and Embodiment 2 can be applied to a communication terminal apparatus.

[Industrial Applicability]

[0073] The reception apparatus and the reception method according to the present invention can prevent saturation and sensitivity degradation of a receiver even when downlink transmit power control is performed and has the advantage of calibrating DC offset voltage without increasing current consumption and is useful in calibrating offset voltage.

[Brief Description of Drawings]

[0074]

FIG.1 is a block diagram showing the configuration of a reception apparatus according to Embodiment 1 of the present invention;

FIG.2 illustrates a block diagram showing the configuration of an analog baseband circuit according to Embodiment 1 of the present invention;

FIG.3 shows the downlink frame configuration in GPRS according to Embodiment 1 of the present invention;

FIG.4 shows the configuration of consecutive time slots of the downlink in GPRS according to Embodiment 1 of the present invention;

FIG.5 is a schematic view showing transmit power control by a base transceiver station in multi-slot transmission according to Embodiment 1 of the present invention;

FIG.6 shows gain distribution by an analog baseband circuit according to Embodiment 1 of the present invention;

FIG.7 shows gain distribution by an analog baseband circuit according to Embodiment 1 of the present invention;

FIG.8 shows the configuration of a time slot in GPRS according to Embodiment 2 of the present invention; and

FIG.9 shows a GSM network configuration;

FIG.10 is a block diagram showing a conventional DC offset

voltage calibration circuit;

[0075]

100 RECEPTION APPARATUS
101 LOW NOISE AMPLIFIER
103 QUADRATURE DEMODULATOR
104 PHASE SHIFTER
105A, 105B ANALOG BASEBAND CIRCUIT
106 DIGITAL SIGNAL PROCESSING SECTION
107 TRANSMIT POWER INFORMATION EXTRACTION SECTION
108 FIELD INTENSITY MEASUREMENT SECTION
109 GAIN SETTING SECTION
110 GAIN CONTROL CIRCUIT
111 VOLTAGE CALIBRATION CIRCUIT

ABSTRACT

[Object] A reception apparatus capable of preventing saturation and sensitivity degradation of a receiver when base transceiver station transmit power control is performed and calibrating offset voltage without increasing the amount of current consumption.

[Overcoming Means] Gain setting section 109 estimates reception field intensity of each time slot in the next frame based on information of the reception field intensity and transmit power information which is information of the transmit power of the base transceiver station and calculates a gain set value according to the estimated reception field intensity. A gain control circuit 110 extracts a maximum gain out of the gains set by the gain setting section 109, uses the maximum gain as a set gain for DC offset voltage calibration and performs gain control at the gain set value corresponding to each time slot.A voltage calibration circuit 111 performs the DC offset voltage calibration of the received signal.

[Selected Drawing] Fig.1

FIG.1

RECEIVED SIGNAL
109 GAIN SETTING SECTION
110 GAIN CONTROL CIRCUIT
105a ANALOG BASEBAND CIRCUIT
111 VOLTAGE CALIBRATION CIRCUIT
105b ANALOG BASEBAND CIRCUIT
108 FIELD INTENSITY MEASUREMENT SECTION
107 TRANSMIT POWER INFORMATION EXTRACTION SECTION
106 DIGITAL SIGNAL PROCESSING SECTION

FIG.2

FROM GAIN CONTROL CIRCUIT 110
FROM MIXER 103a
TO DIGITAL SIGNAL PROCESSING SECTION 106
FROM VOLTAGE CALIBRATION CIRCUIT 111

FIG.3

#303 FIRST FREQUENCY CHANNEL
#304 SECOND FREQUENCY CHANNEL
#305 THIRD FREQUENCY CHANNEL

FIG.5

TRANSMIT POWER INTENSITY
TIME
TIME SLOT
MOBILE STATION

FIG.6

TOTAL GAIN[dB]
GAIN OF VARIABLE GAIN AMPLIFIER 201[dB]
GAIN OF VARIABLE GAIN AMPLIFIER 203[dB]
GAIN OF VARIABLE GAIN AMPLIFIER 205[dB]

FIG.7

TOTAL GAIN[dB]
GAIN OF VARIABLE GAIN AMPLIFIER 201[dB]

GAIN OF VARIABLE GAIN AMPLIFIER 203[dB]
GAIN OF VARIABLE GAIN AMPLIFIER 205[dB]

FIG.9
901 TELEPHONE NETWORK
910, 909 CELL

FIG.10
1006 DIGITAL SIGNAL PROCESSING SECTION
DECODER